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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/626,507
Filing Date: July 24, 2003
Appellant(s): HO ET AL.

Michael D. Wiggins
For Appellant

EXAMINER'S ANSWER

The reply brief filed on June 30, 2008 has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

Response to Argument

Appellant argues that "typically known in the art MAC (media access controller) receives a data packet and routes the data based on an address field in the data packet. Here however it is noted that MAC of Zaidi is a memory access controller and not media access controller known in the art. Appellant further argues that MAC 140 does not selectively receive data based on switching and instead receives all data over a "shared memory bus" 104. Here again it is noted that claims do not recite how the processors are connected to switch (e.g. by individual bus or shared bus), the limitations in the claims (e.g. claim 1) recite:

"a first memory interface that communicates with the first memory device;

a second memory interface that communicates with the second memory device;

a line cache that receives a second address that is based on the first address and includes a memory selection portion; and

a switch that receives the second address and that selectively connects said line cache to one of said first and second memory interfaces based on the memory select portion".

As noted above the claims do not require showing how switch (e.g. MAC) receives that data and also they do not require whether the MAC is connected via a shared bus or not? As shown above, a first memory and a second memory interfaces are required, which is shown in figs. 1, 20, 21, 22 and 23 (e.g. both memories are connected to the MAC means there is a first and second memory interface to connect both the memories. The only limitation needed to show is the switch (e.g. MAC)

selectively connects cache to the first memory or the second memory based on the second address and this limitation is taught by Zaidi at cols. 23 and 24 (e.g. "a switched channel memory controller to allow particular DMAs or CPU to access only certain channels. For example a CPU instruction bus can be connected to an external flash memory through one channel or an external SDRAM memory through anther channel"). Here it is readily apparent that the switched channel MAC 140 selectively connects CPU a flash memory or an external SDRAM, thus satisfying the limitation of the claim. Thus, it is noted that appellant's argument that MAC is connected via shared bus is not valid here. Appellant further argues that a MAC and in particular the MAC 140 as described in Zaidi is not sometimes connected to one device and connected to other device at other times. Instead the MAC 140 appears to be connected to both the devices (e.g. flash 106 and SDRAM 108) at all time via the same interface (i.e. the shared bus 104). Here again noted that the MAC described in the Zaidi is not typically known MAC (media access controller), but is a memory access controller. Also, claims do not require how MAC (e.g. switch) is connected to processors and caches (e.g. via shared bus 104), instead claims merely require a first interface that communicates with first memory and a second interface that communicates with the second memory and a switch that selectively connects said first and second memories to the cache and/or processors and as shown in figs. 21-23 of Zaidi, MAC has separate controls (e.g. flash control and SDRAM control) to connect caches to either flash or the SDRAM, e.g. see fig. 22, I-cache is connected to the flash memory and D-cache is connected to the SDRAM.

Appellant further argues that examiner must show that the alleged structure necessarily (i.e. must) be included. However it is noted that in the rejection, Examiner never noted that the structure is inherent, but instead it is stated that "selection of respective signals are inherent in the system of Zaidi" (e.g. see page 6, lines 1-3 of the office action mailed on May 02, 2007) and the switch can include plurality of selectors, which is known in the art. Therefor it is noted that the Examiner did not said that the structure is inherent in the system of Zaidi, instead the selection of signals were inherent and the switch including plurality of selectors is well known as taught by Jeddeloh.

Thus, it is apparently clear that the appellant is arguing the limitations that are not in the claims and hence the arguments presented in reply brief are not persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kaushik Patel

/Kaushik Patel/

Examiner, AU 2188

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
09/15/08